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For further details

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ACCIDENT IDENTIFICATION SYSTEM USING GPS

SYNOPIS

The objective of this project is to monitor and accident identification using Global Positioning System. The Global Positioning System is a space age navigational system that can pinpoint your position anywhere on the globe, usually within a few yards or meters. This amazing technology is available to everyone, everywhere, day and night, and best of all, at no cost for use of the navigational data. GPS uses a constellation of 24 satellites in precise orbits approximately 11,000 miles above the earth. The satellites transmit data via high frequency radio waves back to Earth and, by locking onto these signals; a GPS receiver can process this data to triangulate its precise location on the globe.

GPS operates 24 hours a day, in all weather conditions, and can be used worldwide for precise navigation on land, on water and even in the air. Some of its many current applications include: boating, fishing, hunting, scouting on land or from the air, hiking, camping, biking, rafting, pack trips by horseback, hot air ballooning, general aviation, snowmobiling and skiing, search and rescue, emergency vehicle tracking, 4 wheeling, highway driving and a host of other outdoor activities where accurate positioning is required.

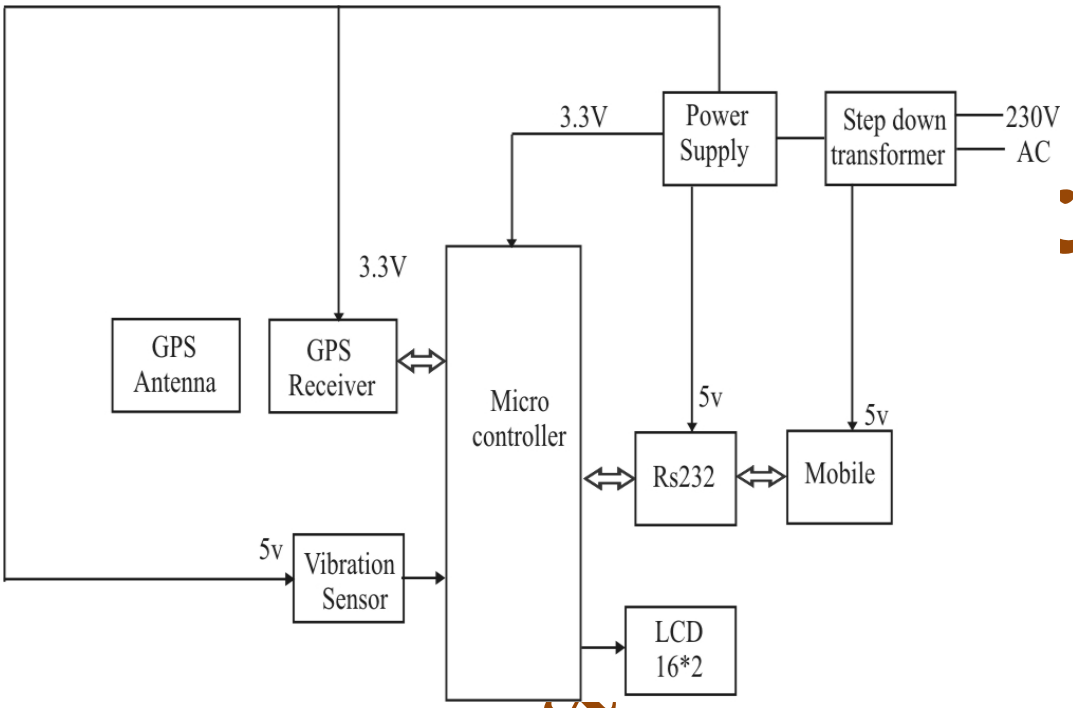
Brief methodology:

This project is designed with

- GPS antenna
- GPS receiver
- Microcontroller
- RS232
- Mobile or GSM modem
- PC
- Vibration sensor
-

In this project GPS is used to monitor the vehicle position any where in the earth. The vehicle who wants to monitor has to have the GPS sensor. The GPS sensor consists of GPS antenna and GPS receiver. GPS uses satellite ranging to triangulate your position. In other words, the GPS unit simply measures the travel time of the signals transmitted from the satellites, then multiplies them by the speed of light to determine exactly how far the unit is from every satellite its sampling. By locking onto the signals from a minimum of three different satellites, a GPS receiver can calculate a 2D (two-dimensional) positional fix, consisting of your latitude and longitude.

BLOCK DIAGRAM:



GPS receiver received vehicle position latitude and longitude from satellite through GPS antenna. GPS receiver is interfaced with the microcontroller through RS232 converter. RS 232 converter is used to convert RS232 logic to TTL logic vice versa because GPS receiver is the RS232 logic and microcontroller is the TTL logic. Then the receiver sends the received signal to microcontroller. Here the microcontroller is the flash type reprogrammable microcontroller in which we have already programmed. Now the microcontroller displays the latitude and longitude on the

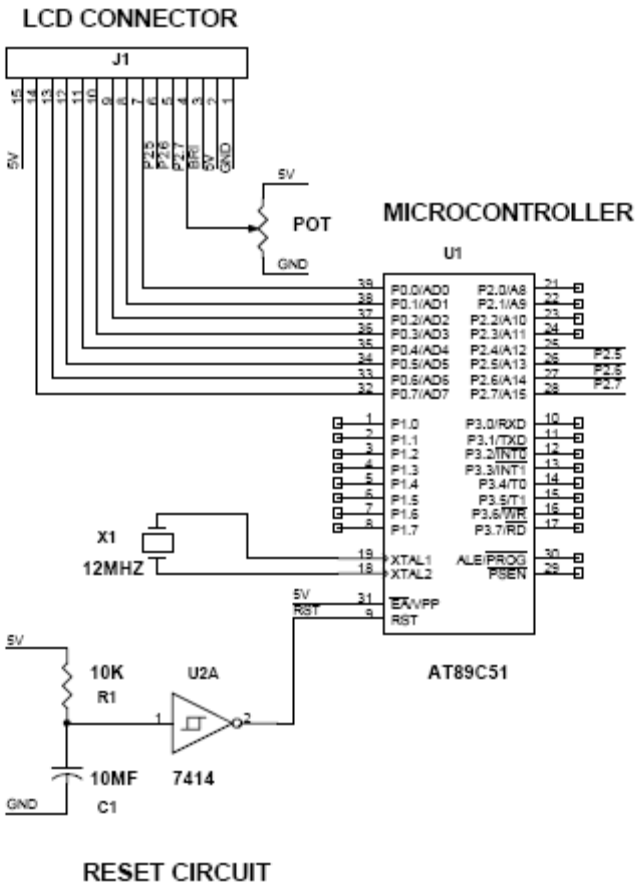
LCD display. Then position information signal is transmitted through GSM network or mobile. The mobile is interfaced with the microcontroller through data cable.

Data cable is the special type of cable which is available with mobile phone. If accident occurs in any place, then the GPS system transmits the current location through mobile. The accident is found through vibration sensor. We can easily track out the accident place by receiving end mobile.

OVERALL DIAGRAM:

DESCRIPTION:

MICROCONTROLLER:



INTRODUCTION

Microcontrollers are destined to play an increasingly important role in revolutionizing various industries and influencing our day to day life more strongly than one can imagine. Since its emergence in the early 1980's the microcontroller has been recognized as a general purpose building block for intelligent digital

systems. It is finding using diverse area, starting from simple children's toys to highly complex spacecraft. Because of its versatility and many advantages, the application domain has spread in all conceivable directions, making it ubiquitous. As a consequence, it has generate a great deal of interest and enthusiasm among students, teachers and practicing engineers, creating an acute education need for imparting the knowledge of microcontroller based system design and development. It identifies the vital features responsible for their tremendous impact, the acute educational need created by them and provides a glimpse of the major application area.

MICROCONTROLLER

A microcontroller is a complete microprocessor system built on a single IC. Microcontrollers were developed to meet a need for microprocessors to be put into low cost products. Building a complete microprocessor system on a single chip substantially reduces the cost of building simple products, which use the microprocessor's power to implement their function, because the microprocessor is a natural way to implement many products. This means the idea of using a microprocessor for low cost products comes up often. But the typical 8-bit microprocessor based system, such as one using a Z80 and 8085 is expensive. Both 8085 and Z80 system need some additional circuits to make a microprocessor system. Each part carries costs of money. Even though a product design may requires only very simple system, the parts needed to make this system as a low cost product.

To solve this problem microprocessor system is implemented with a single chip microcontroller. This could be called microcomputer, as all the major parts are in the IC. Most frequently they are called microcontroller because they are used they are used to perform control functions.

The microcontroller contains full implementation of a standard MICROPROCESSOR, ROM, RAM, I/0, CLOCK, TIMERS, and also SERIAL PORTS. Microcontroller also called "system on a chip" or "single chip microprocessor system" or "computer on a chip".

A microcontroller is a Computer-On-A-Chip, or, if you prefer, a single-chip computer. Micro suggests that the device is small, and controller tells you that the device' might be used to control objects, processes, or events. Another term to describe a microcontroller is embedded controller, because the microcontroller and its support circuits are often built into, or embedded in, the devices they control.

Today microcontrollers are very commonly used in wide variety of intelligent products. For example most personal computers keyboards and implemented with a microcontroller. It replaces Scanning, Debounce, Matrix Decoding, and Serial transmission circuits. Many low cost products, such as Toys, Electric Drills, Microwave Ovens, VCR and a host of other consumer and industrial products are based on microcontrollers.

EVOLUTION OF MICROCONTROROLLER

Markets for microcontrollers can run into millions of units per application. At these volumes of the microcontrollers is a commodity items and must be optimized so that cost is at a minimum. .Semiconductor manufacturers have produced a mind-numbing array of designs that would seem to meet almost any need. Some of the

chips listed in this section are no longer regular production, most are current, and a few are best termed as "smoke ware": the dreams of an aggressive marketing department.

Sl.No	Manufacturer	Chip Designation	Year	No. of Pins	No of I/O	RAM	ROM	Other Features
	4 Bit MC							
1.	Texas Instruments	TMS 1000	Mid 1970	28	23	64	1K	LED Display
2.	Hitachi	HMCS 40	-	28	10	32	512	10 bit ROM
3.	Toshiba	TLCS 47	-	42	35	128	2K	Serial bit I/O
	8 bit MC							
1.	Intel	8048	1976	40	27	64	1K	External Memory 8K
2	Intel	8051	1980	40	32	128	4K	External Memory 128 K
3.	Motorola	6081	1977	-	31	128	2 K	

4.	Motorola	68HC11	1985	52	40	256	8K	Serial Port, ADC,
5.	Zilog	Z8	-	40	32	128	2K	External Memory 128K,
	16 Bit MC							
1.	Intel	80C196	-	68	40	232	8K	External Memory 64K, Serial Port, ADC, WDT, PWM
2.	Hitachi	H8/532	-	84	65	1K	32K	External Memory 1M, Serial Port, ADC, PWM
3.	National	HPC16164	-	68	52	512	16K	External Memory 64K,

								ADC, WDT, PWM
	32 Bit MC							
1.	Intel	80960	-	132	20 MHz clock, 32 bit bus, 512 byte instruction cache			

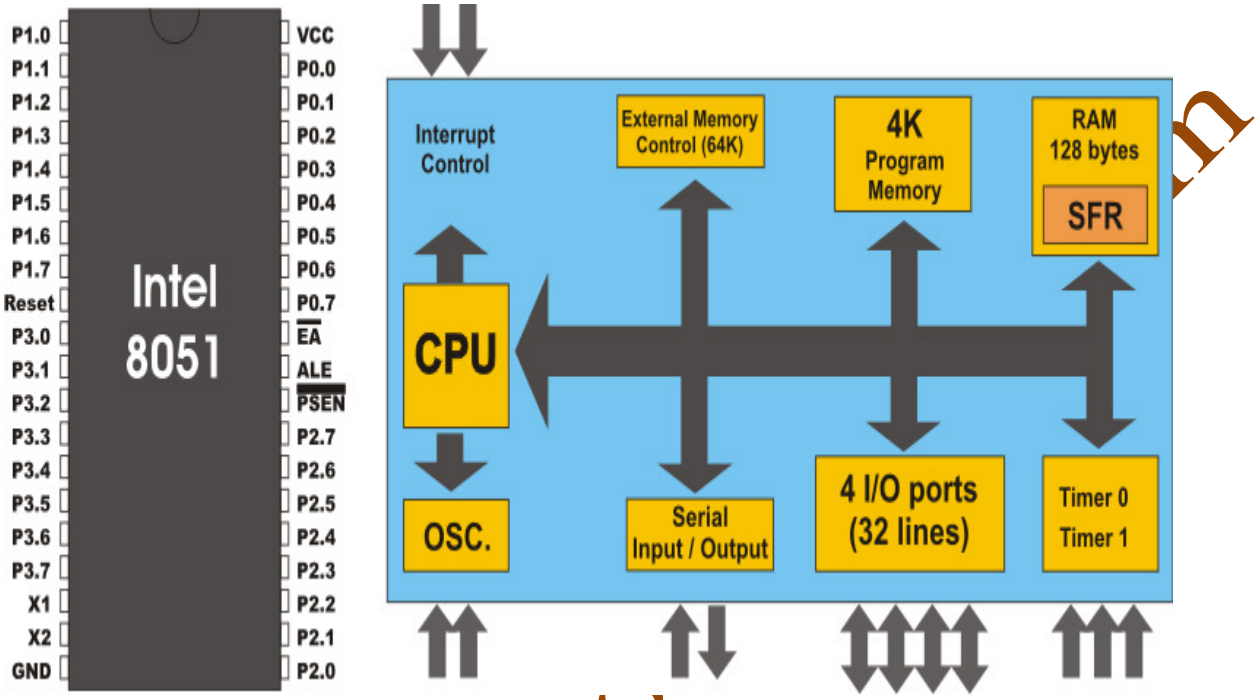
APPLICATION

A microcontroller is a kind of miniature computer that you can find in all kinds of Gizmos. Some examples of common, every-day products that have microcontrollers are built-in. If it has buttons and a digital display, chances are it also has a programmable microcontroller brain.

Every-Day the devices used by ourselves that contain Microcontrollers. Try to make a list and counting how many devices and the events with microcontrollers you use in a typical day. Here are some examples: if your clock radio goes off, and you hit the snooze button a few times in the morning, the first thing you do in your day is interact with a microcontroller. Heating up some food in the microwave oven and making a call on a cell phone also involve operating microcontrollers. That's just the beginning. Here are a few more examples: Turning on the Television with a handheld remote, playing a hand held game, Using a calculator, and Checking your digital wrist watch. All those devices have microcontrollers inside them, that interact with you. Consumer appliances aren't the only things that contain microcontrollers.

Robots, machinery, aerospace designs and other high-tech devices are also built with microcontrollers.

BLOCK AND PIN DIAGRAM OF MICROCONTROLLER



PIN DESCRIPTION

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 may also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit

addresses (MOVX @ DPTR). In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG)

during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

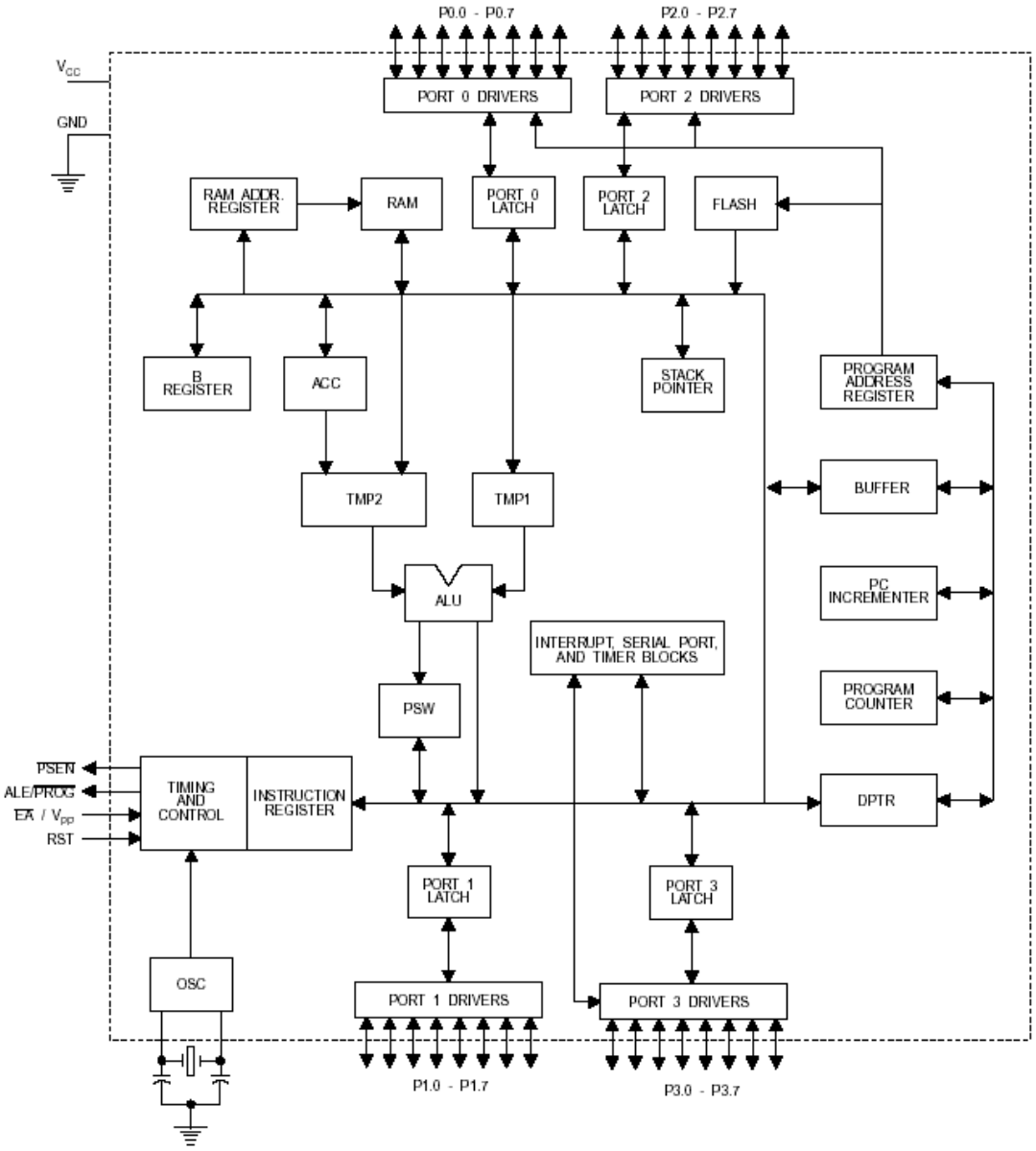
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier. It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm

takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ARCHITECTURE OF 89C51



ADVANTAGES OF MICROCONTROLLERS:

If a system is developed with a microprocessor, the designer has to go for external memory such as RAM, ROM or EPROM and peripherals and hence the size of the PCB will be large enough to hold all the required peripherals. But, the micro controller has got all these peripheral facilities on a single chip so development of a similar system with a micro controller reduces PCB size and cost of the design.

One of the major differences between a micro controller and a microprocessor is that a controller often deals with bits , not bytes as in the real world application, for example switch contacts can only be open or close, indicators should be lit or dark and motors can be either turned on or off and so forth.

INTRODUCTION TO ATMEL MICROCONTROLLER

SERIES: 89C51 Family, **TECHNOLOGY:** CMOS

The major Features of 8-bit Micro controller ATMEL 89C51:

- 8 Bit CPU optimized for control applications
- Extensive Boolean processing (Single - bit Logic) Capabilities.
- On - Chip Flash Program Memory
- On - Chip Data RAM
- Bi-directional and Individually Addressable I/O Lines
- Multiple 16-Bit Timer/Counters
- Full Duplex UART
- Multiple Source / Vector / Priority Interrupt Structure
- On - Chip Oscillator and Clock circuitry.
- On - Chip EEPROM

- SPI Serial Bus Interface
- Watch Dog Timer

POWER MODES OF ATMEL 89C51 ICROCONTROLLER:

To exploit the power savings available in CMOS circuitry. Atmel ’s Flash micro controllers have two software-invited reduced power modes.

IDLE MODE:

The CPU is turned off while the RAM and other on - chip peripherals continue operating. Inn this mode current draw is reduced to about 15 percent of the current drawn when the device is fully active.

POWER DOWN MODE:

All on-chip activities are suspended while the on – chip RAM continues to hold its data. In this mode, the device typically draws less than 15 Micro Amps and can be as low as 0.6 Micro Amps

POWER ON RESET:

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges.

To ensure a valid reset, the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles. On power up, VCC should rise within approximately 10ms. The oscillator start-up time depends on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1ms.With the given circuit, reducing VCC quickly to 0 causes the RST pin voltage to momentarily fall

below 0V. How ever, this voltage is internally l limited and will not harm the device.

MEMORY ORGANIZATION:

* Logical Separation of Program and Data Memory *

All Atmel Flash micro controllers have separate address spaces for program and data memory as shown in Fig 1.The logical separation of program and data memory allows the data memory to be accessed by 8 bit addresses . Which can be more quickly stored and manipulated by an 8 bit CPU Nevertheless 16 Bit data memory addresses can also be generated through the DPTR register.

Program memory can only be read. There can be up to 64K bytes of directly addressable program memory. The read strobe for external program memory is the Program Store Enable Signal (PSEN) Data memory occupies a separate address space from program memory. Up to 64K bytes of external memory can be directly addressed in the external data memory space. The CPU generates read and write signals, RD and WR, during external data memory accesses. External program memory and external data memory can be combined by an applying the RD and PSEN signals to the inputs of AND gate and using the output of the fate as the read strobe to the external program/data memory.

PROGRAM MEMORY:

The map of the lower part of the program memory, after reset, the CPU begins execution from location 0000h. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it executes the service routine. External Interrupt 0 for example, is assigned to location

0003h. If external Interrupt 0 is used, its service routine must begin at location 0003h. If the I interrupt in not used its service location is available as general-purpose program memory.

The interrupt service locations are spaced at 8 byte intervals 0003h for External interrupt 0, 000Bh for Timer 0, 0013h for External interrupt 1,001Bh for Timer1, and so on. If an Interrupt service routine is short enough (as is often the case in control applications) it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations. If other interrupts are in use. The lowest addresses of program memory can be either in the on-chip Flash or in an external memory. To make this selection, strap the External Access (EA) pin to either VCC or GND. For example, in the AT89C51 with 4K bytes of on-chip Flash, if the EA pin is strapped to VCC, program fetches to addresses 0000h through 0FFFh are directed to internal Flash. Program fetches to addresses 1000h through FFFFh are directed to external memory.

DATA MEMORY:

The Internal Data memory is dived into three blocks namely, Refer Fig

- The lower 128 Bytes of Internal RAM.
- The Upper 128 Bytes of Internal RAM.
- Special Function Register

Internal Data memory Addresses are always 1 byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes. Direct addresses higher than 7Fh access one memory space, and indirect addresses higher than 7Fh access a different Memory Space.

The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) Select, which register bank, is in use. This architecture allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16-bytes above the register banks form a block of bit addressable memory space. The micro controller instruction set includes a wide selection of single - bit instructions and this instruction can directly address the 128 bytes in this area. These bit addresses are 00h through 7Fh. either direct or indirect addressing can access all of the bytes in lower 128 bytes. Indirect addressing can only access the upper 128. The upper 128 bytes of RAM are only in the devices with 256 bytes of RAM.

The Special Function Register includes Ports latches, timers, peripheral controls etc., direct addressing can only access these register. In general, all Atmel micro controllers have the same SFRs at the same addresses in SFR space as the AT89C51 and other compatible micro controllers. However, upgrades to the AT89C51 have additional SFRs. Sixteen addresses in SFR space are both byte and bit Addressable. The bit Addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80h through FFh.

ADDRESSING MODES:

DIRECT ADDRESSING:

In direct addressing, the operand specified by an 8-bit address field in the instruction. Only internal data RAM and SFR's can be directly addressed.

INDIRECT ADDRESSING:

In Indirect addressing, the instruction specifies a register that contains the address of the operand. Both internal and external RAM can indirectly address.

The address register for 8-bit addresses can be either the Stack Pointer or R0 or R1 of the selected register Bank. The address register for 16-bit addresses can be only the 16-bit data pointer register, DPTR.

INDEXED ADDRESSING:

Program memory can only be accessed via indexed addressing this addressing mode is intended for reading look-up tables in program memory. A 16 bit base register (Either DPTR or the Program Counter) points to the base of the table, and the accumulator is set up with the table entry number. Adding the Accumulator data to the base pointer forms the address of the table entry in program memory.

Another type of indexed addressing is used in the“ case jump ” instructions. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the Accumulator data.

REGISTER INSTRUCTION:

The register banks, which contains registers R0 through R7, can be accessed by instructions whose opcodes carry a 3-bit register specification. Instructions that access the registers this way make efficient use of code, since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the row bank select bits in PSW.

REGISTER - SPECIFIC INSTRUCTION:

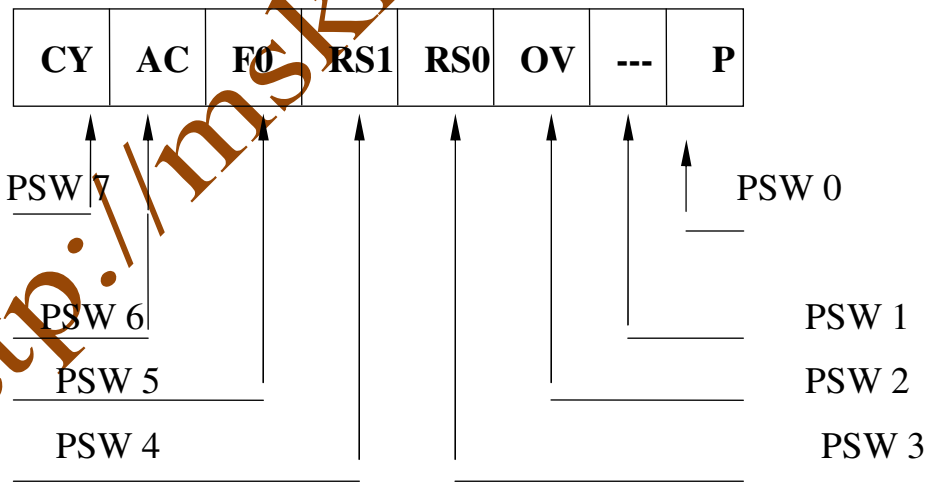
Some Instructions are specific to a certain register. For example some instruction always operates on the Accumulator, so no address byte is needed to point OT ir. In these cases, the opcode itself points to the correct register. Instruction that register to Accumulator as A assemble as Accumulator - specific Opcodes.

IMMEDIATE CONSTANTS:

The value of a constant can follow the opcode in program memory For example. MOV A, #100 loads the Accumulator with the decimal number 100. The same number could be specified in hex digit as 64h.

PROGRAM STATUS WORD:

Program Status Word Register in Atmel Flash Micro controller:



PSW 0:

Parity of Accumulator Set By Hardware To 1 if it contains an Odd number of 1s, Otherwise it is reset to 0.

PSW1:

User Definable Flag

PSW2:

Overflow Flag Set By Arithmetic Operations

PSW3:

Register Bank Select

PSW4:

Register Bank Select

PSW5:

General Purpose Flag.

PSW6:

Auxiliary Carry Flag Receives Carry Out from

Bit 1 of Addition Operands

PSW7:

Carry Flag Receives Carry Out From Bit 1 of ALU Operands.

The Program Status Word contains Status bits that reflect the current sate of the CPU. The PSW shown if Fig resides in SFR space. The PSW contains the Carry Bit, The auxiliary Carry (For BCD Operations) the two - register bank select bits, the Overflow flag, a Parity bit and two user Definable status Flags.

The Carry Bit, in addition to serving as a Carry bit in arithmetic operations also serves the as the "Accumulator" for a number of Boolean Operations .The bits RS0 and RS1 select one of the four register banks. A number of instructions register to these RAM locations as R0 through R7.The status of the RS0 and RS1 bits at execution time determines which of the four banks is selected.

The Parity bit reflect the Number of 1s in the Accumulator .P=1 if the Accumulator contains an even number of 1s, and P=0 if the Accumulator contains an even number of 1s. Thus, the number of 1s in the Accumulator plus P is always even. Two bits in the PSW are uncommitted and can be used as general-purpose status flags.

INTERRUPTS

The AT89C51 provides 5 interrupt sources: Two External interrupts, two-timer interrupts and a serial port interrupts. The External Interrupts INT0 and INT1 can each either level activated or transistion - activated, depending on bits IT0 and IT1 in Register TCON. The Flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to hardware clears the flag that generated an external interrupt *only* if the interrupt WA transition - activated. If the interrupt was level - activated, then the external requesting source (rather than the on-chip hardware) controls the requested flag. Tf0 and Tf1 generate the Timer 0 and Timer 1 Interrupts, which are set by a rollover in their respective Timer/Counter Register (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it when the service routine is vectored to. The logical OR of RI and TI generate the Serial Port Interrupt. Neither of these flag is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI or TI generated the interrupt an the bit must be cleared in software.

In the Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flag is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI to TI generated the interrupt and the bit must be cleared in software.

IE: INTERRUPT ENABLE REGISTER

EA	-	ET2	ES	ET1	EX1	ET0	EX0

Enable bit = 1 enabled the interrupt

Enable bit = 0 disables it.

Symbol	Position	Function
EA	IE.	Global enable / disable all interrupts. If EA = 0, no interrupt will be Acknowledge. If EA = 1, each interrupt source is individually enabled to disabled by setting or clearing its enable bit
-	IE.6	Undefined / reserved
ET2	IE.5	Timer 2 Interrupt enable Bit
ES	IE.4	Serial Port Interrupt enabled bit.
ET1	IE.3	Timer 1 Interrupt enable bit.
EX1	IE.2	External Interrupt 1 enable bit.

ET0	IE.1	Timer 0 Interrupt enable bit.
EX0	IE.0	External Interrupt 0 enable bit.

OSCILLATOR AND CLOCK CIRCUIT:

XTAL1 and XTAL2 are the input and output respectively of an inverting amplifier which is intended for use as a crystal oscillator in the pierce configuration, in the frequency range of 1.2 MHz to 12 MHz. XTAL2 also the input to the internal clock generator.

To drive the chip with an internal oscillator, one would ground XTAL1 and XTAL2. Since the input to the clock generator is divide by two flip flop there are no requirements on the duty cycle of the external oscillator signal. However, minimum high and low times must be observed.

The clock generator divides the oscillator frequency by 2 and provides a tow phase clock signal to the chip. The phase 1 signal is active during the first half to each clock period and the phase 2 signals are active during the second half of each clock period.

CPU TIMING:

A machine cycle consists of 6 states. Each stare is divided into a phase / half, during which the phase 1 clock is active and phase 2 half. Arithmetic and Logical operations take place during phase1 and internal register - to register transfer take place during phase 2

TRENDS AND DEVELOPMENTS IN MICRO CONTROLLER

The manner in which the use of micro controllers is shaping our lives is breathtaking. Today, this versatile device can be found in a variety of control applications. **CVTs, VCRs**, **CD** players, microwave ovens, and automotive engine systems are some of these.

A micro controller unit (MCU) uses the microprocessor as its central processing unit (CPU) and incorporates memory, timing reference, **I/O** peripherals, etc on the same chip. Limited computational capabilities and enhanced **I/O** are special features.

The micro controller is the most essential **IC** for continuous process- based applications in industries like chemical, refinery, pharmaceutical automobile, steel, and electrical, employing programmable logic systems (DCS). **PLC** and **DCS** thrive on the programmability of an **MCU.**

There are many **MCU** manufacturers. To understand and apply general concepts, it is necessary to study one type in detail. This specific knowledge can be used to understand similar features of other **MCU**s.

Micro controller devices have many similarities. When you look at the differences, they are not so great either. Most common and popular **MCU**s are considered to be mature and well-established products, which have their individual adherents and devotees. There are a number of variants within each family to satisfy most memory, **I/O**, data conversion, and timing needs of end-user applications.

The **MCU** is designed to operate on application-oriented sensor data-for example, temperature and pressure of a blast furnace in an industrial process that is fed

through its serial or operated on under the control of software and stored in **ROM**. Appropriate signals are fed via output ports to control external devices and systems.

APPLICATIONS OF MICROCONTROLLERS

Microcontrollers are designed for use in sophisticated real time applications such as

1. Industrial Control
2. Instrumentation and
3. Intelligent computer peripherals

They are used in industrial applications to control

- Motor
- Robotics
- Discrete and continuous process control
- In missile guidance and control
- In medical instrumentation
- Oscilloscopes
- Telecommunication
- Automobiles
- For Scanning a keyboard
- Driving an LCD
- For Frequency measurements
- Period Measurements

GLOBAL POSITIONING SYSTEM:

interface to the communication link. Thanks to the US Government announcement of 911E regulation, radio based position technology has witnessed a spurt of developmental activities.

Network Overlay Systems use cell phone infrastructure for locating vehicles. The cell centers with additional hardware and software assess the time of arrival (TOA) and angle of arrival (AOA) of radio signals from vehicles to compute the position of the vehicles. This information is sent to the tracking centre through the cell link or conventional link. Another technique used for locating vehicles computes the time difference for signals from two cell centers to reach the vehicle. This computation is made in the IVU and the position information is sent to the tracking centre through the cell phone link. A more common technique used is direct radio link (DRL). In this system dedicated radio infrastructure is used along with special IVU to compute vehicle location. However all these techniques impose limitation on the operational area. Alternatively, embedded GPS receivers provide absolute position co-ordinates at any point, without any area restrictions.

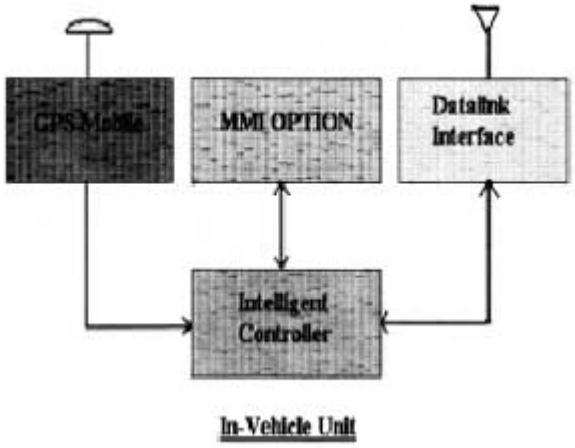
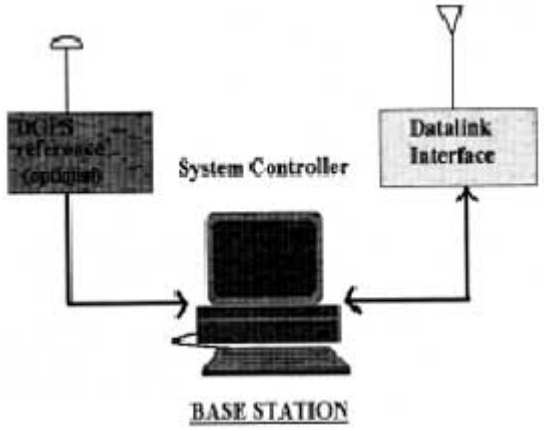


Fig.2 shows the block diagram of an IVU. The controller interacts with the GPS receiver, collects co-ordinates at predefined intervals, processes it and sends out to the communication link. Optionally in certain cases a man-machine- interface like a display with key board can be added for message communication between the driver and the base station.

The base station consists of a high-speed system running VTIS application software that will receive the position data from the vehicles and display on a digital map. It too will have the interface to the communication link. Enhanced features include

video features, trace mode, history track, vehicle database, network support etc. Fig.3 gives the block diagram of a Base station.

The most costly part of a VTIS is the data link. The data link, together with a suitable communication protocol, has to be selected after a thorough study of various parameters such as the bandwidth requirement, number of vehicles to be tracked, expandability, terrain, area of coverage etc. Sophisticated VTIS are linked to data bases that can support information about the vehicles such as the cargo, the temperature of storage of perishable goods, fuel consumption rate etc. Naturally, such systems demand data link with higher bandwidth. UHF links are suitable for short range without shadow region, as they require line of sight. Cell phone based systems demand minimum infrastructure investment, but is limited in coverage. On the contrary, LEO based systems are expensive and offer largest coverage. The recently introduced WAP and GPRS technologies hold great promises for VTIS.



BASE STATION

When multiple vehicles are being tracked, a suitable communication protocol need to be established to avoid collision of radio signal. The simple technique is TDMA, where each IVU communicates during predefined time slots. This synchronization is easy in a GPS based IVU as the GPS receiver provides very precise time reference signal. However, TDMA based systems have limited expandability, flexibility and are known for under-utilization of bandwidth.

The alternative is polling technique. Here each vehicle is addressed by the control station and in response the IVU sends the information. This arrangement enables variable polling rate for different vehicles, non-polling of specific vehicles and expansion of polling list as new vehicles are added.

The relatively large investment needed for the communication link, makes VTIS an opportunity area for service providers. Fig. 4 shows the global market for GPS based

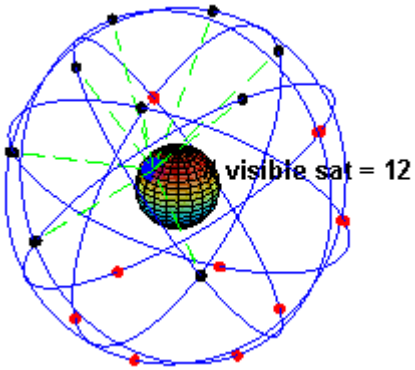
VTIS in the next three years. In US and Europe many vehicle tracking service providers are already in operation. In a large country like India with a very long network of roads and long coastline, this opportunity area is yet to be exploited.

The **Global Positioning System** (**GPS**) is the only fully functional Global Navigation Satellite System (GNSS). Utilizing a constellation of at least 24 Medium Earth Orbit satellites that transmit precise microwave signals, the system enables a GPS receiver to determine its location, speed, direction, and time. Other similar systems are the Russian GLONASS (incomplete as of 2007) and the upcoming European Galileo positioning system

Developed by the United States Department of Defense, GPS is officially named **NAVSTAR GPS** (Contrary to popular belief, NAVSTAR is not an acronym, but simply a name given by Mr. John Walsh, a key decision maker when it came to the budget for the GPS program[1]). The satellite constellation is managed by the United States Air Force 50th Space Wing. The cost of maintaining the system is approximately US$750 million per year,[2] including the replacement of aging satellites, and research and development

Following the shootdown of Korean Air Lines Flight 007 in 1983, President Ronald Reagan issued a directive making the system available for free for civilian use as a common good.[3] Since then, GPS has become a widely used aid to navigation worldwide, and a useful tool for map-making, land surveying, commerce, and scientific uses. GPS also provides a precise time reference used in many applications including scientific study of earthquakes, and synchronization of telecommunications networks.

The current GPS consists of three major segments. These are the space segment



(SS), a control segment (CS), and a user segment

Figure 1

visual example of the GPS constellation in motion with the Earth rotating. Notice how the number of satellites in view from a given point on the Earth's surface, in this example at 45°N, changes with time.

The space segment (SS) comprises the orbiting GPS satellites or Space Vehicles (SV) in GPS parlance. The GPS design originally called for 24 SVs, 8 each in three circular orbital planes, but this was modified to 6 planes with 4 satellites each. The orbital planes are centered on the Earth, not rotating with respect to the distant stars. The six planes have approximately 55° inclination (tilt relative to Earth's equator) and are separated by 60° right ascension of the ascending node (angle along the equator from a reference point to the orbit's intersection).[1] The orbits are arranged so that at least six satellites are always within line of sight from almost everywhere on Earth's surface.

Orbiting at an altitude of approximately 20,200 kilometers (12,600 miles or 10,900 nautical miles; orbital radius of 26,600 km (16,500 mi or 14,400 NM)), each SV makes two complete orbits each sidereal day. The ground track of each satellite therefore repeats each (sidereal) day. This was very helpful during development, since even with just 4 satellites, correct alignment means all 4 are visible from one

spot for a few hours each day. For military operations, the ground track repeat can be used to ensure good coverage in combat zones.

As of September 2007, there are 31 actively broadcasting satellites in the GPS constellation. The additional satellites improve the precision of GPS receiver calculations by providing redundant measurements. With the increased number of satellites, the constellation was changed to a nonuniform arrangement. Such an arrangement was shown to improve reliability and availability of the system, relative to a uniform system, when multiple satellites fail.

GPS broadcast signal

Each GPS satellite continuously broadcasts a **Navigation Message** at 50 bit/s giving the time-of-day, GPS week number and satellite health information (all transmitted in the first part of the message), an *ephemeris* (transmitted in the second part of the message) and an *almanac* (later part of the message). The messages are sent in frames, each taking 30 seconds to transmit 1500 bits.

The first 6 seconds of every frame contains data describing the satellite clock and its relationship to GPS system time. The next 12 seconds contain the **ephemeris** data, giving the satellite's own precise orbit. The ephemeris is updated every 2 hours and is generally valid for 4 hours, with provisions for updates every 6 hours or longer in non-nominal conditions. The time needed to acquire the ephemeris is becoming a significant element of the delay to first position fix, because, as the hardware becomes more capable, the time to lock onto the satellite signals shrinks, but the ephemeris data requires 30 seconds (worst case) before it is received, due to the low data transmission rate.

GPS ANTENNA

We're interested in designing, building, and testing a GPS antenna that would be implemented on the body or inside of a vehicle. This antenna would be different than others on the market in that it would not only utilize the L1 frequency (1575.42 MHz), but also the L5 frequency (1176.45 MHz) to be introduced in the future. Our goal is to also make it interoperable with the European counterpart to GPS, Galileo which uses 1164–1214 MHz and 1563–1591 MHz bands. In addition, we intend to gather the specifications for the LNA that would be needed for our specific antenna based on its gain, impedance, and other characteristics. If time allows, we intend to design and simulate the LNA using Agilent's Advanced Design System software package at the end as well.

Benefits:

- Antenna could be used presently because it would be utilizing the presently available L1 frequency
- L5 frequency will allow compatibility with the modernized GPS system in the future
- Be interoperable with the Galileo system so receiver would be capable of working with that system once it's fully online and functional
- Receiver would need only one antenna for both L1 and L5 frequencies

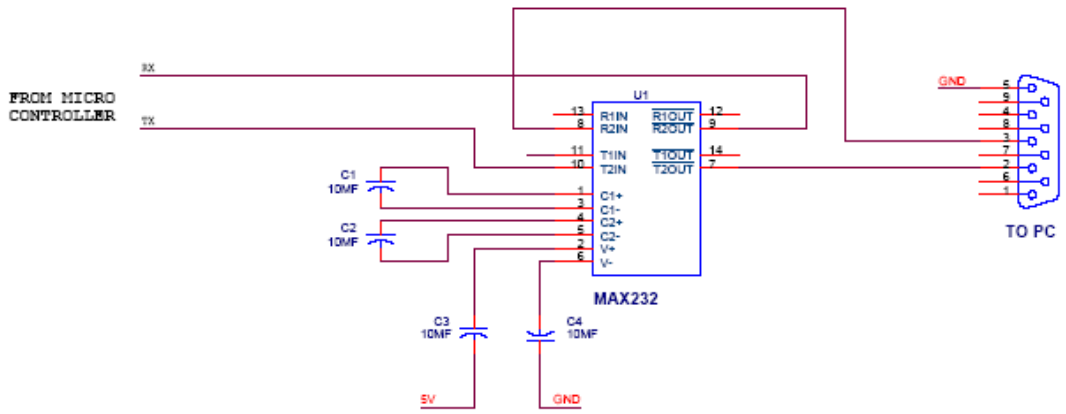
Features:

- Ability to receive both the presently available L1 frequency and the L5 frequency to be introduced in the future

- Interoperability with the Galileo system would allow receiver manufacturer to utilize this antenna

Vehicle mounting of antenna would allow navigational tracking capability for any vehicle

RS232 COMMUNICATION:



RS232:

In telecommunications, **RS-232** is a standard for serial binary data interconnection between a *DTE* (Data terminal equipment) and a *DCE* (Data Circuit-terminating Equipment). It is commonly used in computer serial ports.

Scope of the Standard:

The Electronic Industries Alliance (EIA) standard RS-232-C [3] as of 1969 defines:

- Electrical signal characteristics such as voltage levels, signaling rate, timing and slew-rate of signals, voltage withstand level, short-circuit behavior, maximum stray capacitance and cable length
- Interface mechanical characteristics, pluggable connectors and pin identification
- Functions of each circuit in the interface connector
- Standard subsets of interface circuits for selected telecom applications

The standard does not define such elements as character encoding (for example, ASCII, Baudot or EBCDIC), or the framing of characters in the data stream (bits per character, start/stop bits, parity). The standard does not define protocols for error detection or algorithms for data compression.

The standard does not define bit rates for transmission, although the standard says it is intended for bit rates lower than 20,000 bits per second. Many modern devices can exceed this speed (38,400 and 57,600 bit/s being common, and 115,200 and 230,400 bit/s making occasional appearances) while still using RS-232 compatible signal levels.

Details of character format and transmission bit rate are controlled by the serial port hardware, often a single integrated circuit called a UART that converts data from parallel to serial form. A typical serial port includes specialized driver and receiver

integrated circuits to convert between internal logic levels and RS-232 compatible signal levels.

Circuit working Description:

In this circuit the MAX 232 IC used as level logic converter. The MAX232 is a dual driver/receiver that includes a capacive voltage generator to supply EIA 232 voltage levels from a single 5v supply. Each receiver converts EIA-232 to 5v TTL/CMOS levels. Each driver converts TLL/CMOS input levels into EIA-232 levels.

Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

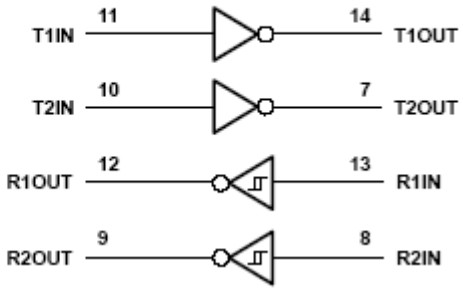
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

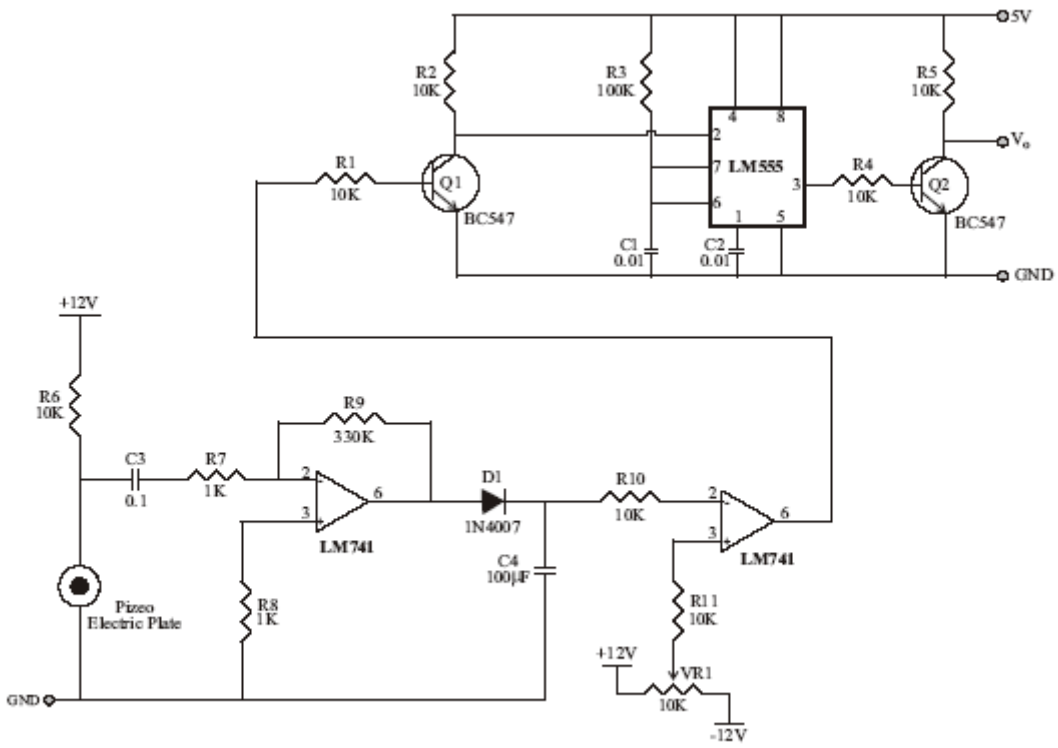
logic diagram (positive logic)



In this circuit the microcontroller transmitter pin is connected in the MAX232 T2IN pin which converts input 5v TTL/CMOS level to RS232 level. Then T2OUT pin is connected to reviver pin of 9 pin D type serial connector which is directly connected to PC.

In PC the transmitting data is given to R2IN of MAX232 through transmitting pin of 9 pin D type connector which converts the RS232 level to 5v TTL/CMOS level. The R2OUT pin is connected to receiver pin of the microcontroller. Likewise the data is transmitted and received between the microcontroller and PC or other device vice versa.

VIBRATION

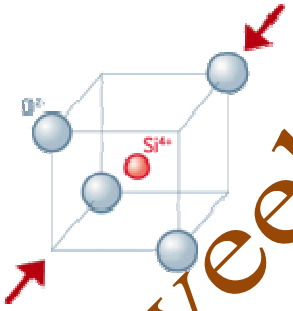


Piezo Electric Sensor:

A piezoelectric sensor is a device that uses the piezoelectric effect to measure pressure, acceleration, strain or force by converting them to an electrical signal.

Piezo Electric Effect:

Piezoelectricity is the ability of crystals and certain ceramic materials to generate a voltage in response to applied mechanical stress. Piezoelectricity was discovered by Pierre Curie and the word is derived from the Greek *piezein*, which means to squeeze or press.



The piezoelectric effect is reversible in that piezoelectric crystals, when subjected to an externally applied voltage, can change shape by a small amount. (For instance, the deformation is about 0.1% of the original dimension in PZT.) The effect finds useful applications such as the production and detection of sound, generation of high voltages, electronic frequency generation, microbalance, and ultra fine focusing of optical assemblies.

Application:

Piezoelectric sensors have proven to be versatile tools for the measurement of various processes. They are used for quality assurance, process control and process development in many different industries.

Piezo electric sensors are also seen in nature. Bones act as force sensors. Once loaded, bones produce charges proportional to the resulting internal torsion or displacement. Those charges stimulate and drive the build up of new bone material. This leads to the strengthening of structures where the internal displacements are the

greatest. With time, this causes weaker structures to increase their strength and stability as material is laid down proportional to the forces affecting the bone.

Circuit Description:

Vibration circuit is used to sense the mechanical vibration. This circuit is constructed with

1. Piezo electric plate.
2. Operational amplifier
3. 555 IC timer

Piezo electric plate is the special type of sensor which is used to sense the mechanical vibration. Piezo electric plate converts the mechanical vibration to electrical signal. The converted electrical signal is in the range of small milli voltage signal.

Then the electrical signal voltage is given to amplifier unit through 0.1uf capacitor in order to filter the noise signal. The amplifier circuit is constructed with operational amplifier LM 741. The amplified output is in the form of AC signal the diode is used to rectify the negative signal.

The rectified signal is given to comparator. The comparator circuit is constructed with LM 741 operational amplifier in which the signal is given to inverting input terminal. The reference voltage is given to non inverting input terminal. It converts the input signal to +12V to -12V square pulse.

The square pulse is given to base of BC 547 transistor whenever the positive side of square pulse is come the transistor conducts emitter and collector side is short circuited because the transistor is act as switch. The collector side is connected to trigger terminal of the 555 IC. When the transistor is conducted negative signal is given to trigger terminal because the emitter is connected to ground side.

Now the 555 IC conducts and generates the square pulse. The frequency of the square pulse is depends upon the resistor and capacitor connected in between 7th (discharge) and 6th (threshold) terminal.

The square pulse is given to base of the Q2 transistor. The transistor is turn ON and turn OFF depends upon the square pulse. The Q2 transistor output is 0 to 5V pulse.

Whenever the Piezo electric plate sense the vibration the Q2 transistor outputs the 0 to 5V pulse. This pulse is given to microcontroller or other related circuit to inform that vibration has been occurred.

POWER SUPPLIES:

INTRODUCTION:

The present chapter introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig 19.1. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified

voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

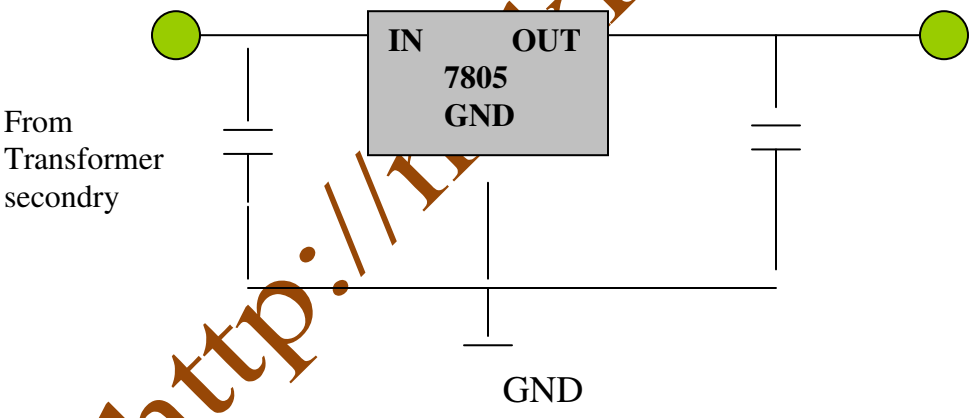
A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering

with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

THREE-TERMINAL VOLTAGE REGULATORS:

Fig shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

Fixed Positive Voltage Regulators:



The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure 19.26 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated + 12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over

some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs is provided in table

Positive Voltage Regulators in 7800 series

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

LCD DISPLAY:

INTRODUCTION:

Liquid crystal displays (LCDs) have materials which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

An LCD consists of two glass panels, with the liquid crystal material sand witched in between them. The inner surface of the glass plates are coated with transparent electrodes which define the character, symbols or patterns to be displayed polymeric layers are present in between the electrodes and the liquid crystal, which makes the liquid crystal molecules to maintain a defined orientation angle.

One each polarisers are pasted outside the two glass panels. These polarisers would rotate the light rays passing through them to a definite angle, in a particular direction.

When the LCD is in the off state, light rays are rotated by the two polarisers and the liquid crystal, such that the light rays come out of the LCD without any orientation, and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes, the liquid crystal molecules would be aligned in a specific direction. The light rays passing through the LCD

would be rotated by the polarisers, which would result in activating / highlighting the desired characters.

The LCD's are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations.
The LCD's don't generate light and so light is needed to read the display. By using backlighting, reading is possible in the dark. The LCD's have long life and a wide operating temperature range.

Changing the display size or the layout size is relatively simple which makes the LCD's more customer friendly.

The LCDs used exclusively in watches, calculators and measuring instruments are the simple seven-segment displays, having a limited amount of numeric data. The recent advances in technology have resulted in better legibility, more information displaying capability and a wider temperature range. These have resulted in the LCDs being extensively used in telecommunications and entertainment electronics. The LCDs have even started replacing the cathode ray tubes (CRTs) used for the display of text and graphics, and also in small TV applications.

POWER SUPPLY:

The power supply should be of +5V, with maximum allowable transients of 10mv. To achieve a better / suitable contrast for the display, the voltage (VL) at pin 3 should be adjusted properly.

A module should not be inserted or removed from a live circuit. The ground terminal of the power supply must be isolated properly so that no voltage is induced in it. The module should be isolated from the other circuits, so that stray voltages are not induced, which could cause a flickering display.

HARDWARE:

Develop a uniquely decoded 'E' strobe pulse, active high, to accompany each module transaction. Address or control lines can be assigned to drive the RS and R/W inputs.

Utilize the Host's extended timing mode, if available, when transacting with the module. Use instructions, which prolong the Read and Write or other appropriate data strobes, so as to realize the interface timing requirements.

If a parallel port is used to drive the RS, R/W and 'E' control lines, setting the 'E' bit simultaneously with RS and R/W would violate the module's set up time. A separate instruction should be used to achieve proper interfacing timing requirements.

MOUNTING:

Cover the display surface with a transparent protective plate, to protect the polarizer. Don't touch the display surface with bare hands or any hard materials. This will stain the display area and degrade the insulation between terminals.

Do not use organic solvents to clean the display panel as these may adversely affect tape or with absorbant cotton and petroleum benzene.

The processing or even a slight deformation of the claws of the metal frame will have effect on the connection of the output signal and cause an abnormal display.

Do not damage or modify the pattern wiring, or drill attachment holes in the PCB. When assembling the module into another equipment, the space between the module and the fitting plate should have enough height, to avoid causing stress to the module surface.

Make sure that there is enough space behind the module, to dissipate the heat generated by the ICs while functioning for longer durations.

When an electrically powered screwdriver is used to install the module, ground it properly.

While cleaning by a vacuum cleaner, do not bring the sucking mouth near the module. Static electricity of the electrically powered driver or the vacuum cleaner may destroy the module.

ENVIRONMENTAL PRECAUTIONS:

Operate the LCD module under the relative condition of 40°C and 50% relative humidity. Lower temperature can cause retardation of the blinking speed of the display, while higher temperature makes the overall display discolor.

When the temperature gets to be within the normal limits, the display will be normal. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and humidity.

Contact with water or oil over a long period of time may cause deformation or colour fading of the display. Condensation on the terminals can cause electro-chemical reaction disrupting the terminal circuit.

TROUBLE SHOOTING

INTRODUCTION:

When the power supply is given to the module, with the pin 3 (VL) connected to ground, all the pixels of a character gets activated in the following manner:

All the characters of a single line display, as in CDM 16108.

The first eight characters of a single line display, operated in the two-line display mode, as in CDM 16116.

The first line of characters of a two-line display as in CDM 16216 and 40216. The first and third line of characters of a four-line display operated in the two-line display mode, as in CDM 20416.

If the above mentioned does not occur, the module should be initialized by software. Make sure that the control signals 'E' , R/W and RS are according to the interface timing requirements.

IMPROPER CHARACTER DISPLAY:

When the characters to be displayed are missing between, the data read/write is too fast. A slower interfacing frequency would rectify the problem.

When uncertainty is there in the start of the first characters other than the specified ones are rewritten, check the initialization and the software routine.

In a multi-line display, if the display of characters in the subsequent lines does'nt take place properly, check the DD RAM addresses set for the corresponding display lines.
When it is unable to display data, even though it is present in the DD RAM, either the display on/off flag is in the off state or the display shift function is not set properly. When the display shift is done simultaneous with the data writa operation, the data may not be visibl on the display.

If a character not found in the font table is displayed, or a character is missing, the CG ROM is faulty and the controller IC have to be changed.

If particular pixels of the characters are missing, or not getting activated properly, there could be an assembling problem in the module.

In case any other problems are encountered you could send the module to our factory for testing and evaluation.

CRYSTALONICS DISPLAY

INTRODUCTION:

Crystalonics dot –matrix (alphanumeric) liquid crystal displays are available in TN, STN types, with or without backlight. The use of C-MOS LCD controller and driver ICs result in low power consumption. These modules can be interfaced with a 4-bit or 8-bit micro processor /Micro controller.

The built-in controller IC has the following features:

- Correspond to high speed MPU interface (2MHz)
- 80 x 8 bit display RAM (80 Characters max)
- 9,920 bit character generator ROM for a total of 240 character fonts. 208 character fonts (5 x 8 dots) 32 character fonts (5 x 10 dots)
- 64 x 8 bit character generator RAM 8 character generator RAM 8 character fonts (5 x 8 dots) 4 characters fonts (5 x 10 dots)
- Programmable duty cycles
  1/8 – for one line of 5 x 8 dots with cursor
  1/11 – for one line of 5 x 10 dots with cursor
  1/16 – for one line of 5 x 8 dots with cursor
- Wide range of instruction functions display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift.
- Automatic reset circuit, that initializes the controller / driver ICs after power on.

FUNCTIONAL DESCRIPTION OF THE CONTROLLER IC

REGISTERS:

The controller IC has two 8 bit registers, an instruction register (IR) and a data register (DR). The IR stores the instruction codes and address information for

display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written, but not read by the MPU.

The DR temporally stores data to be written to /read from the DD RAM or CG RAM. The data written to DR by the MPU, is automatically written to the DD RAM or CG RAM as an internal operation.

When an address code is written to IR, the data is automatically transferred from the DD RAM or CG RAM to the DR. data transfer between the MPU is then completed when the MPU reads the DR. likewise, for the next MPU read of the DR, data in DD RAM or CG RAM at the address is sent to the DR automatically. Similarly, for the MPU write of the DR, the next DD RAM or CG RAM address is selected for the write operation.

The register selection table is as shown below:

RS	R/W	Operation
0	0	IR write as an internal operation
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

BUSY FLAG:

When the busy flag is1, the controller is in the internal operation mode, and the next instruction will not be accepted.

When RS = 0 and R/W = 1, the busy flag is output to DB7.

The next instruction must be written after ensuring that the busy flag is 0.

ADDRESS COUNTER:

The address counter allocates the address for the DD RAM and CG RAM read/write operation when the instruction code for DD RAM address or CG RAM address setting, is input to IR, the address code is transferred from IR to the address counter. After writing/reading the display data to/from the DD RAM or CG RAM, the address counter increments/decrements by one the address, as an internal operation. The data of the address counter is output to DB0 to DB6 while R/W = 1 and RS = 0.

DISPLAY DATA RAM (DD RAM)

The characters to be displayed are written into the display data RAM (DD RAM), in the form of 8 bit character codes present in the character font table. The extended capacity of the DD RAM is 80 x 8 bits i.e. 80 characters.

CHARATCER GENERATOR ROM (CG ROM)

The character generator ROM generates 5 x 8 dot 5 x 10 dot character patterns from 8 bit character codes. It generates 208, 5 x 8 dot character patterns and 32, 5 x 10 dot character patterns.

CHARACTER GENERATOR RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 10 dots, four character patterns can be written.

INTERFACING THE MICROPROCESSOR / CONTROLLER:

The module, interfaced to the system, can be treated as RAM input/output, expanded or parallel I/O.

Since there is no conventional chip select signal, developing a strobe signal for the enable signal (E) and applying appropriate signals to the register select (RS) and read/write (R/W) signals are important.

The module is selected by gating a decoded module – address with the host – processor's read/write strobe. The resultant signal, applied to the LCDs enable (E) input, clocks in the data.

The 'E' signal must be a positive going digital strobe, which is active while data and control information are stable and true. The falling edge of the enable signal enables the data / instruction register of the controller. All module timings are referenced to specific edges of the 'E' signal. The 'E' signal is applied only when a specific module transaction is desired.

The read and write strobes of the host, which provides the 'E' signals, should not be linked to the module's R/W line. An address bit which sets up earlier in the host's machine cycle can be used as R/W.

When the host processor is so fast that the strobes are too narrow to serve as the 'E' pulse

a. Prolong these pulses by using the hosts 'Ready' input
b. Prolong the host by adding wait states
c. Decrease the Hosts Crystal frequency.

Inspite of doing the above mentioned, if the problem continues, latch both the data and control information and then activate the 'E' signal

When the controller is performing an internal operation he busy flag (BF) will set and will not accept any instruction. The user should check the busy flag or should provide a delay of approximately 2ms after each instruction.

The module presents no difficulties while interfacing slower MPUs.

The liquid crystal display module can be interfaced, either to 4-bit or 8-bit MPUs.

For 4-bit data interface, the bus lines DB4 to DB7 are used for data transfer, while DB0 to DB3 lines are disabled. The data transfer is complete when the 4-bit data has been transferred twice.

The busy flag must be checked after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

For 8-bit data interface, all eight-bus lines (DB0 to DB7) are used.

PCB DESIGN:

Design and Fabrication of Printed circuit boards

INTRODUCTION:

Printed circuit boards, or PCBs, form the core of electronic equipment domestic and industrial. Some of the areas where PCBs are intensively used are computers, process control, telecommunications and instrumentation.

MANUFATCURING:

The manufacturing process consists of two methods; print and etch, and print, plate and etch.

The single sided PCBs are usually made using the print and etch method. The double sided plate through – hole (PTH) boards are made by the print plate and etch method.

The production of multi layer boards uses both the methods. The inner layers are printed and etch while the outer layers are produced by print, plate and etch after pressing the inner layers.

SOFTWARE:

The software used in our project to obtain the schematic layout is MICROSIM.

PANELISATION:

Here the schematic transformed in to the working positive/negative films. The circuit is repeated conveniently to accommodate economically as many circuits as possible in a panel, which can be operated in every sequence of subsequent steps in the PCB process. This is called penalization. For the PTH boards, the next operation is drilling.

DRILLING:

PCB drilling is a state of the art operation. Very small holes are drilled with high speed CNC drilling machines, giving a wall finish with less or no smear or epoxy, required for void free through hole plating.

PLATING:

The heart of the PCB manufacturing process. The holes drilled in the board are treated both mechanically and chemically before depositing the copper by the electro less copper platting process.

ETCHING:

Once a multiplayer board is drilled and electro less copper deposited, the image available in the form of a film is transferred on to the out side by photo printing using a dry film printing process. The boards are then electrolyticaly plated on to the circuit pattern with copper and tin. The tin-plated deposit serves an etch resist when copper in the unwanted area is removed by the conveyorised spray etching machines with chemical etchants. The etching machines are attached to an automatic dosing equipment, which analyses and controls etchants concentrations.

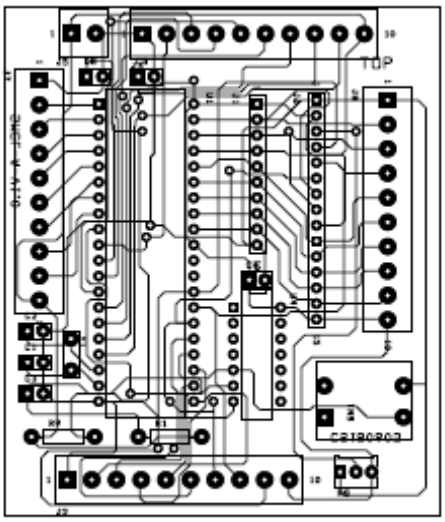
SOLDERMASK:

Since a PCB design may call for very close spacing between conductors, a solder mask has to be applied on the both sides of the circuitry to avoid the bridging of conductors. The solder mask ink is applied by screening. The ink is dried, exposed to UV, developed in a mild alkaline solution and finally cured by both UV and thermal energy.

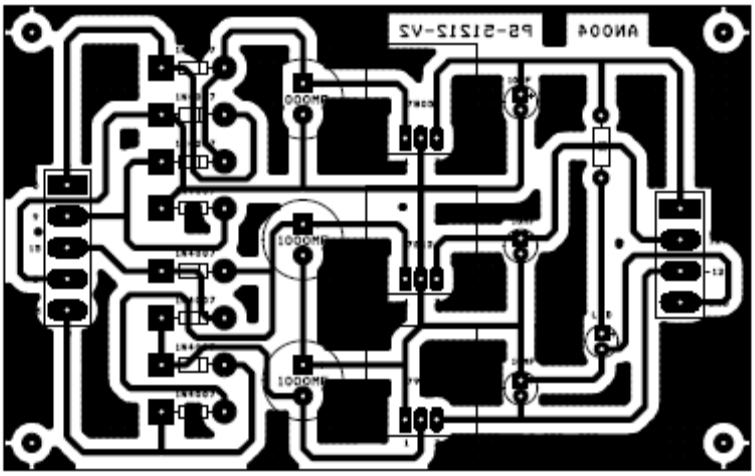
HOT AIR LEVELLING:

After applying the solder mask, the circuit pads are soldered using the hot air leveling process. The bare bodies fluxed and dipped in to a molten solder bath. While removing the board from the solder bath, hot air is blown on both sides of the board through air knives in the machines, leaving the board soldered and leveled. This is one of the common finishes given to the boards. Thus the double sided plated through whole printed circuit board is manufactured and is now ready for the components to be soldered.

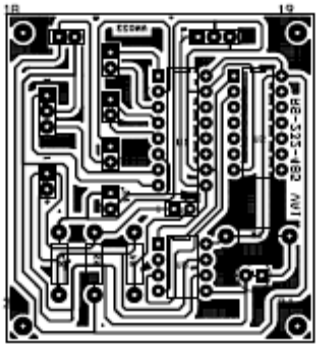
MICROCONTROLLER:



POWER SUPPLY:



RS-232:



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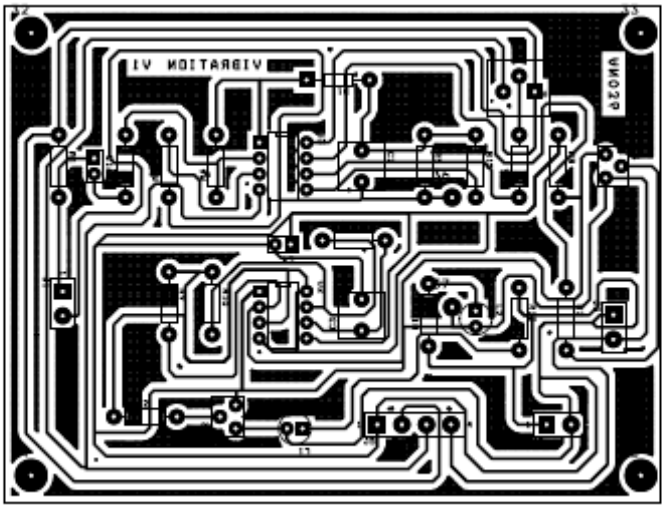

SOFTWARE TOOL:

KEIL C COMPILER:

Keil development tools for the 8051 Microcontroller Architecture support every level of software developer from the professional applications engineer to the student just learning about embedded software development.

The industry-standard Keil C Compilers, Macro Assemblers, Debuggers, Real-time Kernels, Single-board Computers, and Emulators support all 8051 derivatives and help you get your projects completed on schedule

The Keil 8051 Development Tools are designed to solve the complex problems facing embedded software developers.

- When starting a new project, simply select the microcontroller you use from the Device Database and the µVision IDE sets all compiler, assembler, linker, and memory options for you.

- Numerous example programs are included to help you get started with the most popular embedded 8051 devices.

- The Keil µVision Debugger accurately simulates on-chip peripherals (I²C, CAN, UART, SPI, Interrupts, I/O Ports, A/D Converter, D/A Converter, and PWM Modules) of your 8051 device.

- Simulation helps you understand hardware configurations and avoids time wasted on setup problems. Additionally, with simulation, you can write and test applications before target hardware is available.

- When you are ready to begin testing your software application with target hardware, use the MON51, MON390, MONADI, or FlashMON51 Target Monitors, the ISD51 In-System Debugger, or the ULINK USB-JTAG Adapter to download and test program code on your target system.

It's been suggested that there are now as many embedded systems in everyday use as there are people on planet Earth. Domestic appliances from washing machines to TVs, video recorders and mobile phones, now include at least one embedded processor. They are also vital components in a huge variety of automotive, medical, aerospace and military systems. As a result, there is strong demand for programmers with 'embedded' skills, and many desktop developers are moving into this area.

Embedded C is designed for programmers with desktop experience in C, C++ or Java who want to learn the skills required for the unique challenges of embedded systems.

The book and CD-ROM include the following key features:

Simulator:

The Keil hardware simulator for the popular 8051 microcontroller is on the CD-ROM so that readers can try out examples from the book - and create new ones - without requiring additional hardware.

All code is written in C, so no assembly language is required. Industry-standard C compiler from Keil software is included on the CD-ROM, along with copies of code examples from the book to get you up and running very quickly.

Key techniques required in all embedded systems are covered in detail, including the control of port pins and the reading of switches.
A complete embedded operating system is presented, with full source code on the CD-ROM.

Achieve outstanding application performance on Intel processors using Intel® C Compiler for Windows*, including support for the latest Intel multi-core processors. For out-of-the-box productivity, Intel C Compiler plugs into the Microsoft Visual Studio* development environment for IA-32 and features a preview plug-in to the Microsoft Visual Studio .NET environment

This chapter provides information about the C compiler, including operating environments, standards conformance, organization of the compiler, and C-related programming tools.

There are a number of tools available to aid in developing, maintaining, and improving your C programs. The two most closely tied to C, c scope and lint, are described in this book. In addition, a man page exists for each of these tools. Refer to the preface of this book for a list of all the associated man pages.

PROGRAM:

Advantage:

1. Low power consumption.
2. We can easily monitor the vehicle any where in the earth
3. Very high accuracy.

Applications:

Using the GPS receiver, you can determine your location with great precision GPS receivers can be hand carried or installed on aircraft, ships, tanks, submarines, cars, and trucks. These receivers detect, decode, and process GPS satellite signals.

1. This project is mainly used for military application in order to find the terrorist activities.
2. In Police department to find the thieves.
3. Detective department.

CONCLUSION

The progress in science & technology is a non-stop process. New things and new technology are being invented. As the technology grows day by day, we can imagine about the future in which thing we may occupy every place.

The proposed system based on Atmel microcontroller is found to be more compact, user friendly and less complex, which can readily be used in order to perform. Several tedious and repetitive tasks. Though it is designed keeping in mind about the need for industry, it can extended for other purposes such as commercial & research applications. Due to the probability of high technology (Atmel microcontroller) used this "**ACCIDENT IDENTIFICATION SYSTEM USING GPS**" is fully software controlled with less hardware circuit. The feature makes this system is the base for future systems.

The principle of the development of science is that "nothing is impossible". So we shall look forward to a bright & sophisticated world.

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